

IN THE CLAIMS:

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1. A slave device for use in a master-slave system, comprising:
a clock node to receive a clock signal;
5 a phase-to-master node to receive a phase-to-master phase signal; and
a phase-from-master node to receive a phase-from master phase signal.
 2. The slave device of claim 1 wherein said slave device includes a delay-locked
loop to process said clock signal and said phase-to-master signal to produce a transmit
10 clock signal.
 3. The slave device of claim 2 wherein said slave device includes transmit
circuitry to transmit data to a data bus in response to said transmit clock signal.
 - 15 4. The slave device of claim 1 wherein said slave device includes a delay-locked
loop to process said clock signal and said phase-from-master signal to produce a
receive clock signal.
 5. The slave device of claim 4 wherein said slave device includes receive circuitry
20 to receive data from a data bus in response to said receive clock signal.
 6. The slave device of claim 1 wherein said slave device processes a single-ended
phase-to-master phase signal.
 - 25 7. The slave device of claim 1 wherein said slave device processes a single-ended
phase-from-master phase signal.
 8. A master-slave system, comprising:
a clock signal generator to produce a clock signal;
30 a phase signal generator to produce a phase signal;
a clock line connected to said clock signal generator to carry said clock signal;

a phase line connected to said phase signal generator to carry said phase signal, said phase line including a phase-to-master path to carry a phase-to-master phase signal and a phase-from-master path to carry a phase-from-master phase signal;

a master device connected to said clock line and said phase line;

5 a data bus connected to said master device; and

a slave device connected to said data bus, said clock line and said phase line, said slave device processing data on said data bus in response to said clock signal and said phase signal.

10 9. The master-slave system of claim 8 wherein said phase signal generator includes a divide-by-N circuit to produce said phase signal from said clock signal.

10. The master-slave device of claim 8 wherein said clock and phase signal generator includes a pseudo-random number generator to produce said phase signal
15 from said clock signal.

11. The master-slave device of claim 8 wherein said slave device includes a delay-locked loop to process said clock signal and said phase-to-master signal to produce a transmit clock signal
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12. The master-slave device of claim 11 wherein said slave device includes transmit circuitry to transmit data to said data bus in response to said transmit clock signal.

25 13. The master-slave device of claim 8 wherein said slave device includes a delay-locked loop to process said clock signal and said phase-from-master signal to produce a receive clock signal.

14. The master-slave device of claim 13 wherein said slave device includes receive
30 circuitry to receive data from said data bus in response to said receive clock signal.

15. The master-slave device of claim 8 wherein said phase signal has an effective frequency that is lower than the frequency of said clock signal.

16. The master-slave device of claim 8 wherein said phase signal is non-periodic.

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17. A method of operating a master-slave system, said method comprising the steps of:

generating a clock signal and a phase signal, said phase signal including a phase-to-master signal and a phase-from-master signal;

10 transmitting data to a master device in response to said clock signal and said phase-to-master signal; and

receiving data from said master device in response to said clock signal and said phase-from-master signal.

15 18. The method of claim 17 wherein said transmitting data comprises:

producing a transmit clock signal having a frequency determined by said clock signal and said phase-to-master signal.

19. The method of claim 18 wherein said transmitting data comprises:

20 operating data transmit circuitry in response to said transmit clock signal.

20. The method of claim 17 wherein said receiving data comprises:

producing a receive clock signal having a frequency determined by said clock signal and said phase-from-master signal.

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21. The method of claim 20 wherein said receiving data comprises:

operating receive circuitry in response to said receive clock.

22. The method of claim 17 wherein said generating step includes the step of

30 generating said phase signal from said clock signal.

23. The method of claim 22 wherein said generating step includes the step of generating said phase signal as a divided clock signal.

24. The method of claim 22 wherein said generating step includes the step of
5 generating said phase signal as a pseudo-random function of said clock signal.

25. The method of claim 22 wherein said phase signal has an effective frequency that is lower than the frequency of said clock signal.

10 26. The method of claim 22 wherein said phase signal is non-periodic.

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